LISTING OF THE CLAIMS

1-44. (Canceled).

45. (Previously presented) A semiconductor device comprising:

an insulating layer;

an opening in said insulating layer, said opening having sidewalls and a bottom, said bottom being substantially free of polymer residue and silicon rich oxide residue; and

a conductor in said opening.

46. (Previously presented) An integrated circuit comprising:

an ammonia-cleaned High Aspect Ratio opening provided in an insulating layer, said opening being formed over a polysilicon region and a bottom of said opening being substantially free of polymer residue and silicon rich oxide residue; and

a conductor within said opening, said conductor being electrically connected with said polysilicon region.

47. (Previously Presented) An integrated circuit as in claim 46 further comprising a silicide layer between said conductor and said polysilicon region.

48. (Original) An integrated circuit as in claim 46, wherein said integrated circuit is a memory circuit.

49. (Original) An integrated circuit as in claim 47 wherein the interface area between said conductor and polysilicon region is free of oxygen contamination.